STUDENT-DESIGNED BLUETOOTH RADIO IN SILICON-ON-SAPPHIRE

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Abstract **The core of a fully-integrated Bluetooth receiver has been designed in a 0.5um Silicon-on-Sapphire (SOS) process by a team of 11 students during the Spring 2000 semester. Unlike previously reported RFIC development work done by graduate students in the course of their research, this design was completed in the context of a classroom setting in a single semester. The receiver incorporates a number of research efforts underway at the authors' institution, providing a wide range of students with exposure to state-of-the-art design methods. Details of both the class structure and of the Bluetooth architecture being studied are discussed. Measurements taken from an early prototype circuit in SOS are also reported**.

I. Introduction

The ability of universities to design significant RF integrated circuits has been demonstrated many times. For example, in [1] and [2], a team of approximately 12 graduate students, postdocs, and professors describe a complete single-chip 900 MHz spread-spectrum transceiver built in a 1 um bulk-CMOS process. Many smaller-scale RFIC development efforts carried out between graduate students and faculty have been reported in conference proceedings and journals over the past decade. However, there has been little work reported on designing large-scale ICs in a classroom setting, or with the involvement of undergraduate students.

This paper describes such an effort carried out at Kansas State University, in which the goal was to design, simulate, and tapeout a fully-integrated Bluetooth receiver IC within a single semester. The class, which combines research and educational objectives, is an outgrowth of a series of courses in which K-State students have worked in large teams to design significant products [3]. The structure of these courses is outlined, followed by a description of the Bluetooth product designed during the Spring 2000 semester. Simulated and measured results of key circuits used in the design are also presented and pointers to class web pages are provided for those interested in additional details.

II. Receiver Architecture

Courses of this type can be run in a manner similar to an industry design job. For example, a system-engineer is needed to define the overall product architecture so that it conforms to various specifications. In the case of a Bluetooth receiver, specifications include sensitivity, adjacent and alternate channel selectivity, out-of-band blocking, and maximum usable input level [4]. Derived specifications for actual circuits such as noise figure, compression and intercept points, and filter rejection must then be determined, based on a particular receiver architecture being proposed. Making these decisions, as well as partitioning the project into blocks and assigning them to specific individuals typically falls to the most experienced engineer(s), which in the context of a class, is the instructor. In this course, the architecture shown in Figure 1 was chosen based on "corporate history" (experience with, and research interest in certain technologies) at our school.

This design was developed during the first half of the semester as students learned background material required for implementating the detailed circuit designs needed for realization. Unlike direct-conversion and low-IF architectures being applied elsewhere [5], this design is based on the classic superhet approach. Thus, it retains many of the desirable features of superhet receiver implementations. However, it is unique in several ways.

First, the design relies on unusual on-chip RF filtering technology in which the traditional preselect filter, LNA, and image filter combination is replaced by a single, integrated, "Q-enhanced LNA" [6]. The combined LNA/filter has a nominal bandwidth of 20 MHz, which is less than the band of interest. Hence, it acts as a tuned-preselect filter, providing improved protection against strong interferers. The filter is step-tuned to one of 6 center frequencies according to the channel to be received, and is followed by an image reject mixer downconverting to a first IF of 120.5 MHz (nominal) where final tuning takes place. Total image rejection in the RF to 1st IF conversion exceeds 50 dB with this design, and attenuation of out-of-band inteferrers is superior to direct-conversion designs that do not provide preselect filtering in fully-integrated implementations [6].

Final channel selection is done at the 1st IF to 2nd IF downconversion (from 120.5 MHz to 5.5 MHz) using a low-power synthesizer at 126 MHz (nominal). The 1st IF to 2nd IF downconversion relies on a second IR mixer and no image reject filtering is provided at this stage. While

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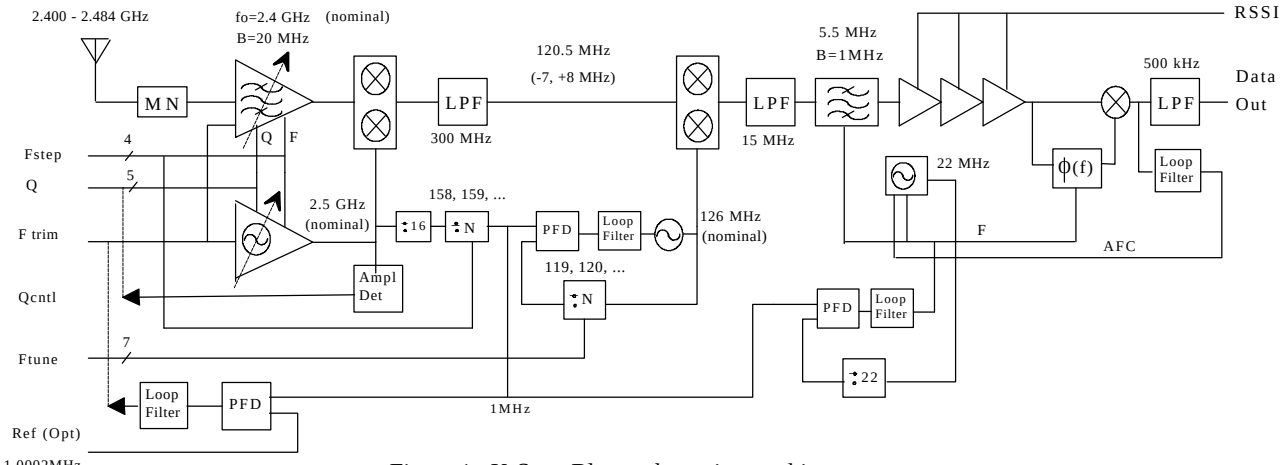

Figure 1. K-State Bluetooth receiver architecture.

generally unwise, considering the limited rejection of IR mixers, the Bluetooth spec allows for low attenuation of in-band images, making such strategies possible.

Finally, the receiver employs classical analog channel-select filtering and demodulation techniques. A 5.5 MHz 2nd IF frequency combined with the 1 MHz Bluetooth channel allows a bandpass gm-C filter to be implemented at low power with straightforward master-slave tuning of frequency only. A quadrature phase-shift FM demod employs a copy of the gm-C resonator used in the filter, and is followed by a 3-pole LPF for 11 MHz product and noise attenuation prior to bit decisions, while a limiting IF amplifier with RSSI circuit complete the design. Control lines shown on the left side of the figure are used to implement frequency hopping and master-slave tuning. These are assumed to be interfaced to a host microcontroller, which was not included in the class project.

This architecture was developed to meet all performance specs for Bluetooth, and the overall power budget needed to meet dynamic range constraints within the filters, mixers, and amplifiers was calculated as 15 mA (although many students exceeded their power budget by up to 50%).

II. Background Technology

Since two primary goals of the course were to introduce students to ongoing research activities in RFIC development, and to allow the students to participate in those activties, a portion of the classroom lectures covered research in Q-enhanced filter design being carried out at our school. Such filters have been shown to be viable for on-chip bandpass application with fractional bandwidths as low as 1 percent of center frequency [6], but to-date have not been incorporated into commercial designs. Problems remaining to be solved include developing robust tuning techniques and achieving high dynamic range with acceptable power consumption.

Solving both problems requires a fabrication process in which a spiral inductor Q of at least 8 to 10 can be achieved. To address this need, we selected a Silicon-on-Sapphire (SOS) technology available through MOSIS and prototyped circuits in the technology prior to the first offering of the course. These circuits included a simple one-pole Q-enhanced BPF at 900 MHz as shown in the die photo of Figure 2.

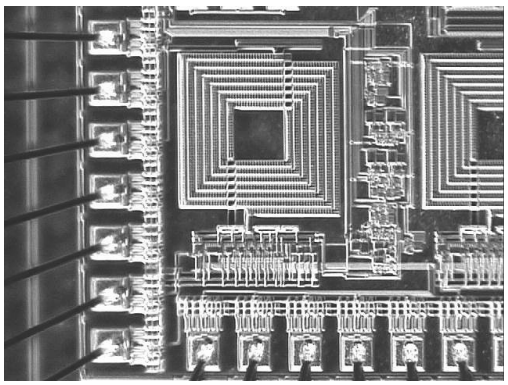

Figure 2. Photo of Q-enhanced filter prototyped in SOS.

The purpose of this prototype was to gain experience in the process and to validate theoretical predictions of dynamic range that can be achieved at low power. Previous Q-enhanced filters operating at 900 MHz with a selectivity bandwidth of 20 MHz have achieved a 1dB-compression dynamic range figure of 75 dB (relative to a 1MHz channel bandwidth) [6], but at the cost 39 mA per pole. This high power is due to the low starting Q of 3 available in bulk CMOS. Since power consumption in Q-enhanced filters scales inversely with the square of the inductor Q [6], an SOS-based filter with an inductor Q of 8 and a similar dynamic range should consume

significantly less power. The filter prototyped here achieved a 1dB compression dynamic range of 77 dB with approximately 12 mA current consumption, in general keeping with theory. Moreover, spurious-free dynamic range relative to out-of-band signals measured 71dB with tones at 40 and 80 MHz offsets, and 77 dB with 80 and 160 MHz offsets, confirming previously reported out-of-band performance advantages of the technology over unprotected LNAs [6].

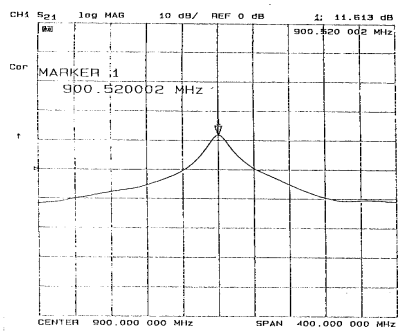

Figure 3. Nominal filter response with Q enhanced for 20 MHz bandwidth.

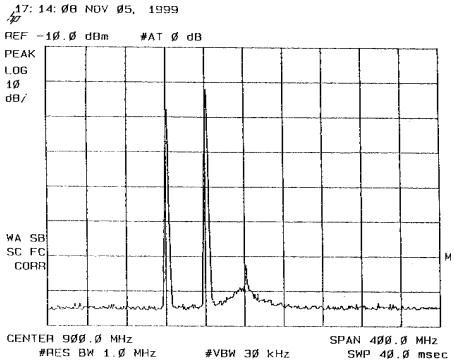

Figure 4. Filter output noise floor and response to out-of-band interferrers at -20 dBm input.

III. Design Partitioning and Student Assignments

For significant design projects such as the development of a complete Bluetooth receiver IC, the instructor of a product-design oriented class should assume the tasks of partitioning the overall design into subcircuits or blocks that can be developed by individual students. Partitioning the design is best handled after collecting "resumes" early in the semester, so students can be assigned to sections of the design in which they have both an interest and appropriate background. This generally provides the best chance for a successful project completion.

Keeping the project on-schedule requires careful crafting of each assignment to guide the students through major tasks, while falling short of making detailed design decisions for them. This is perhaps the most time-consuming part of preparing and running such a class, but is essential if students are to remain on-track throughout the semester [3].

In the Bluetooth receiver development course, resumes were collected early in the semester while the first several weeks were being devoted to lectures covering system design and core circuits. Core circuits included differential amplifiers, spiral inductors and their performance limitations, LC tuned-RF amplifiers and oscillators, Gm-C filters/oscillators, and image reject mixers that would be needed in the project. System level design issues including gain and noise budgeting, impedance levels at the interface between design blocks, and special features of the SOS process used, were also discussed. The overall block diagram was then partitioned into the following subtasks to be implemented by individual students:

- Integrated Dipole Antenna
- Integrated Loop Antenna
- Q-Enhanced LNA and Local Oscillator
- Master-Slave Tuning Components
- 2.5 GHz Dynamic and 700 MHz Static Flip-Flops
- High Speed Programmable Divider, PFD, and Charge pump
- First and Second Image Reject Mixers
- Second LO
- 2-pole IF Channel-Select Filter
- IF amp and RSSI
- FSK demod and 3-pole Lowpass Filter

III. Results

The project was kept on-track through a sequence of four assignments, requiring students to develop preliminary designs, detailed schematics, layouts, and finally, layout-vs-schematic (LVS) checks. These were graded and given back immediately after the due date to keep the project on a tight schedule. For their final exam, students were then required to document their work in the form of web pages. Examples of material posted on these pages are shown in Figures 5 and 6. This design is an improved, lower-power version of the prototype Q-enhanced LNA previously discussed, and includes master-slave tuning. The simulation results of Figure 6 validate the tracking of the filter's frequency response to the master oscillator (which doubles as the 1st downconversion's LO).

Similar schematics and simulations together with circuit descriptions, layouts, and LVS checks are posted on each student's page and are available for reference by other researchers and future classes [7]. The final layout shown in Figure 7 contains all students' circuits, with the

exception of the integrated antennas which were determined to have insufficient efficiency at the wavelength and frequency of the 2.4 GHz ISM band. This layout was submitted for fabrication at the first scheduled run of the process after the end of the semester, and finished Silicon (and Sapphire) will be available in time to be tested at the next course offering during the Spring 2001 semester.

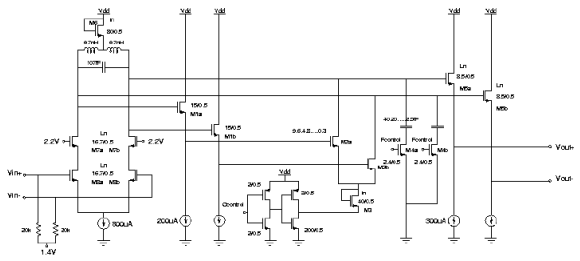

Figure 5. Q-enhanced filter schematic.

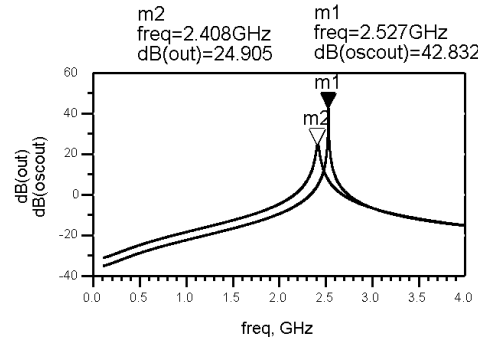

Figure 6. Simulation of master-slave tracking.

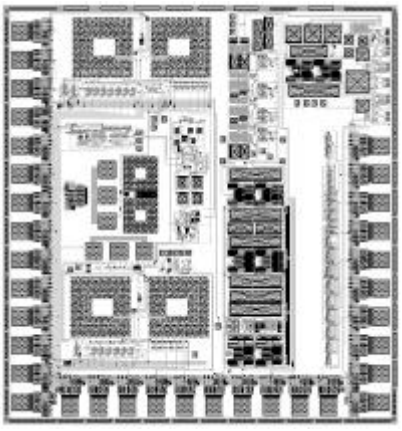

Figure 7. Final IC layout.

V. Conclusions and Future Directions

Combining research and education in a product-design class has many benefits for both students and instructor. First, the teamwork and large-scale development efforts help to engage the students' enthusiasm, providing an effective hands-on (active) learning style. This motivates students to learn the material better, and in some cases has helped encourage them to continue their studies to the Masters program, where they might otherwise have been tempted by the lure of high starting salaries immediately following their BS degree. In addition, the course has been successful in furthering and expanding our research efforts. The design described here contains several concepts and circuits that will help in the study and development of RFICs in general and Q-enhanced filters and Bluetooth products in particular. In a follow-on course offered in the Spring 2001 semester, we will continue these efforts by testing and refining the design describe here, and by developing a companion transmitter to form a complete Bluetooth physical layer solution.

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